DATE: 12 August, 2021

PCN #: 2540

PCN Title: Qualified Additional Fab Site, Assembly/Test (A/T) Sites, Bill of Material (BOM) and updated Device Data Sheets

Dear Customer:

This is an announcement of change(s) to products that are currently being offered by Diodes Incorporated.

We request that you acknowledge receipt of this notification within 30 days of the date of this PCN. If you require samples for evaluation purposes, please make a request within 30 days as well. Otherwise, samples may not be built prior to this change. Please refer to the implementation date of this change as it is stated in the attached PCN form. Please contact your local Diodes sales representative to acknowledge receipt of this PCN and for any sample requests.

The changes announced in this PCN will not be implemented earlier than 90 days from the notification date stated in the attached PCN form.

Previously agreed upon customer specific change process requirements or device specific requirements will be addressed separately.

For questions or clarification regarding this PCN, please contact your local Diodes sales representative.

Sincerely,

Diodes Incorporated PCN Team

## PRODUCT CHANGE NOTICE PCN-2540 REV 1

| Notification Date: | Implementation Date: | Product Family: | Change Type: | PCN #: |
|---|---|---|---|---|
| 12 August, 2021 | 12 November, 2021 | Analog Semiconductors | Fab Site, A/T Sites, BOM and Data Sheet Change | **2540** |

**TITLE**

Qualified Additional Fab Site, Assembly/Test (A/T) Sites, Bill of Material (BOM) and updated Device Data Sheets

**DESCRIPTION OF CHANGE**

This PCN is being issued to notify customers that in order to assure continuity of supply, Diodes has qualified additional Fab Site Dongbu HiTek (FAB2) located in Eumseong-gun, South Korea, Diodes Internal A/T Site (CAT) located in Chengdu, China, additional A/T Site Greatek Electronics Inc. (GTK Zhunan) located in Zhunan, Taiwan, additional A/T Site (SIMAT) located in Shanghai, China, and additional A/T Site JCET Group Co., Ltd. (JCET) located in Suqian, China. In addition, we have qualified PdCu wire, EMG-350 Mold Compound, second source lead frame supplier (LeFram) and data sheet changes on selected devices.

Full electrical characterization and high reliability testing has been completed on representative part numbers to ensure no change to device functionality or electrical specifications in the datasheet. Refer to the attached qualification report embedded in this file (to view, download this PCN file then open it with a PDF viewer to see the attached qual report).

**IMPACT**

Continuity of Supply. There will be no change to the Form, Fit or Function of products affected, unless specifically indicated.

**PRODUCTS AFFECTED**

Table 1 - Qualified Additional Mold Compound (EMG-350)
Table 2 - Qualified Additional Fab Site (DBH FAB2 Eumseong-gun)
Table 3 - Qualified Additional A/T Site (GTK Zhunan)
Table 4 - Qualified Additional A/T Site (JCET Suqian)
Table 5 - Qualified Additional Lead Frame Supplier (LeFram)
Table 6 - Qualified Additional A/T Site (SIMAT)
Table 7 - Qualified Additional Bump Site * (LBS), Additional A/T Site (CAT) to include PdCu Bond Wire
Table 8 - Update Datasheet Specifications (See Table 8A for Data Sheet Comparison)

**WEB LINKS**

| | |
|---|---|
| **Manufacturer's Notice:** | https://www.diodes.com/quality/product-change-notices/diodes-product-change-notices/ |
| **For More Information Contact:** | https://www.diodes.com/about/contact-us/contact-sales/ |
| **Data Sheet:** | https://www.diodes.com/catalog/ |

**DISCLAIMER**

**Unless a Diodes Incorporated Sales representative is contacted in writing within 30 days of the posting of this notice, all changes described in this announcement are considered approved.**

**Table 1 - Qualified Additional Mold Compound (EMG-350)**

| | | | | | |
|---|---|---|---|---|---|
| AP3706P-G1 | | | | | |

| Table 2 - Qualified Additional Fab Site (DBH FAB2 Eumseong-gun) | | | | | |
|---|---|---|---|---|---|
| AP62300TWU-7 | AP62300WU-7 | | | | |

| Table 3 - Qualified Additional A/T Site (GTK Zhunan) | | | | | |
|---|---|---|---|---|---|
| PI90LV01TEX | PI90LV02TEX | | | | |

| Table 4 - Qualified Additional A/T Site (JCET Suqian) | | | | | |
|---|---|---|---|---|---|
| PI3CH400ZBEX | PI4ULS3V204ZBEX | PI4ULS5V104ZBEX | | | |

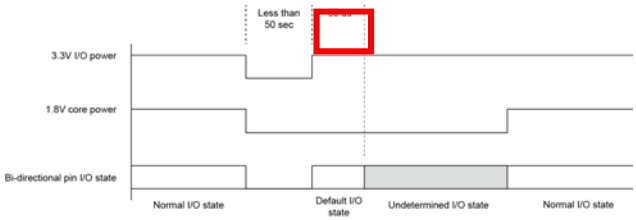
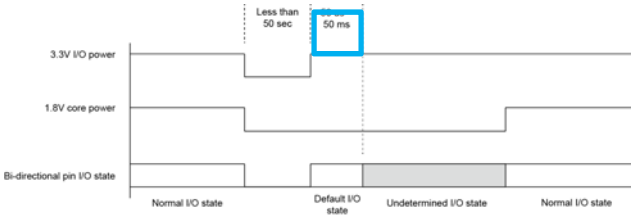
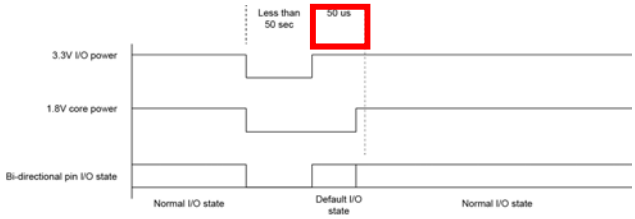
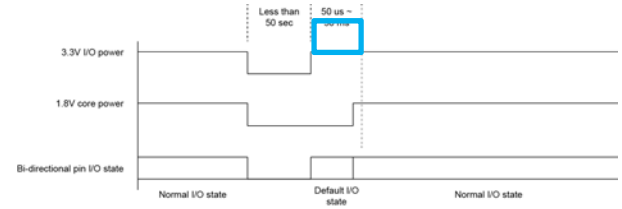
| Table 5 - Qualified Additional Lead Frame Supplier (LeFram) | | | | | |
|---|---|---|---|---|---|
| PI49FCT3805DHEX | PI49FCT38072BHEX | PI49FCT3807DHEX | PI6C10810HEX | | |

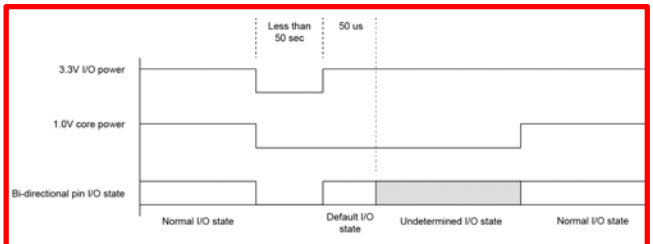
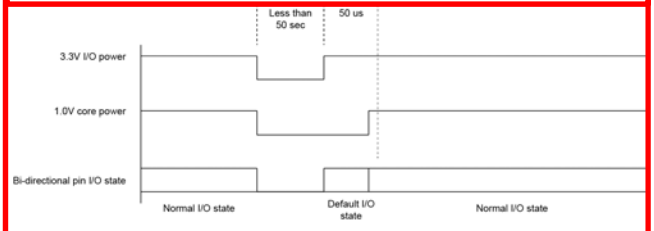
| Table 6 - Qualified Additional A/T Site (SIMAT) | | | | | |
|---|---|---|---|---|---|
| AP4310AMTR-AG1 | AP4310AMTR-AG1-01 | AP4310AMTR-G1 | AP4310AMTR-G1-73 | AP4310AMTR-G1-C01 | AP4310AUMTR-AG1 |
| AP4310AUMTR-G1 | AP4310EMTR-AG1 | AP4310EMTR-G1 | DAS01B | | |

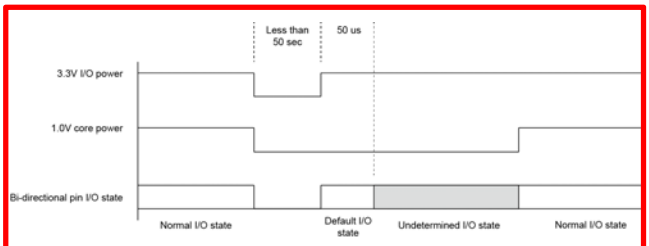
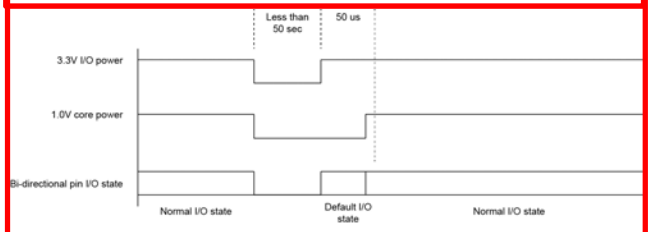
| Table 7 - Qualified Additional Bump Site * (LBS), Additional A/T Site (CAT) to include PdCu Bond Wire | | | | | |
|---|---|---|---|---|---|
| AP2337SA-7 | AP2501M8-13 | AP63300WU-7* | AP63301WU-7* | AP7361-18SP-13 | AP7362-10SP-13 |
| AP7362-12SP-13 | AP7362-15SP-13 | AP7362-18SP-13 | AP7362-25SP-13 | AP7362-33SP-13 | AP7362A-10SP-13 |
| AP7362A-12SP-13 | AP7362A-15SP-13 | AP7362A-18SP-13 | AP7362A-25SP-13 | AP7362A-33SP-13 | AP7362A-SP-13 |
| AP7362-SP-13 | AP7363-SP-13 | | | | |

| Table 8 - Update Data Sheet Specifications (See Table 8A for Data Sheet Comparison) | | | | | |
|---|---|---|---|---|---|
| PI7C9X110BNBE | PI7C9X111SLBFDE | PI7C9X111SLBFDE-2017 | PI7C9X111SLBFDEX | PI7C9X111SLBFDEX-2017 | PI7C9X112SLFDE |
| PI7C9X112SLFDEX | PI7C9X113SLFDE | PI7C9X113SLFDE-2017 | PI7C9X113SLFDEX | PI7C9X113SLFDEX-2017 | PI7C9X118SLFDE |
| PI7C9X118SLFDEX | PI7C9X130DNDE | | | | |

## Table 8A: Data Sheet Comparison (Following 8 pages)

| Current Data Sheet | New Data Sheet |
|---|---|
| 16 POWER SEQUENCING | 16 POWER SEQUENCING |
| The PI7C9X110B require two voltages: 3.3V I/O voltage and 1.8V core voltage. The 1.8V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X110B, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.8V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X110B will not be damaged as long as 3.3V is applied either before or at the same time as 1.8V. | The PI7C9X110B require two voltages: 3.3V I/O voltage and 1.8V core voltage. The 1.8V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X110B, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.8V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X110B will not be damaged as long as 3.3V is applied either before or at the same time as 1.8V. |
| During power cycle, if there is a delay in applying 1.8V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause the device totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states. | During power cycle, if there is a delay in applying 1.8V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause the device totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states. |
| The typical time for PI7C9X110B to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Certain precautions should be made if the delay between 3.3V and 1.8V is larger than 50us. Figure 16-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 16-2 shows the recommended power sequence timing. | The typical time for PI7C9X110B to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Figure 16-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 16-2 shows the recommended power sequence timing. |
|  |  |
| **Figure** Error! No text of specified style in document.**-1 Timing Sequence with Undetermined I/O State** | **Figure** Error! No text of specified style in document.**-3 Timing Sequence with Undetermined I/O State** |
|  |  |
| **Figure** Error! No text of specified style in document.**-2 Recommended Power Sequence** | **Figure** Error! No text of specified style in document.**-4 Recommended Power Sequence** |
| When 1.8V core power is applied after 3.3V IO power is applied, there might be glitch at reset pins (PERST_L and RESET_L), and an external RC filter can be used to filter out the glitch if necessary. | If the gap between 3.3V IO power and 1.8V core power is too big, there might be glitch at pins PERST_L and RESET_L. The maximum gap is recommended to be 50us~50ms, customer needs to measure the waveform of PERST_L and RESET_L to make sure there is no glitch during the gap. |

| Current Data Sheet | New Data Sheet |
|---|---|
| 15 POWER SEQUENCING<br>The PI7C9X111SL requires two voltages: 3.3V I/O voltage and 1.0V core voltage. The 1.0V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X111SL, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.0V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X111SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.0V.<br><br>During power cycle, if there is a delay in applying 1.0V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause the device totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states.<br><br>The typical time for PI7C9X111SL to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Certain precautions should be made if the delay between 3.3V and 1.0V is larger than 50us. Figure 15-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 15-2 shows the recommended power sequence timing.<br><br>  <br>**Figure** Error! No text of specified style in document.**-5 Timing sequence with undetermined I/O state**<br><br>  <br>**Figure** Error! No text of specified style in document.**-6 Recommended Power Sequence**<br><br>When 1.0V core power is applied after 3.3V IO power is applied, there might be glitch at reset pins (PERST_L and RESET_L), and an external RC filter can be used to filter out the glitch if necessary. | 15 POWER SEQUENCING<br>The PI7C9X111SL requires two voltages: 3.3V I/O voltage and 1.0V core voltage. The 1.0V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X111SL, the user can either apply all voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.0V) within the suggested maximum delay (50ms). If all power rails are not applied at the same time, the PI7C9X111SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.0V. |

| Current Data Sheet | New Data Sheet |
|---|---|
| 14 POWER SEQUENCING<br>The PI7C9X112SL requires two voltages: 3.3V I/O voltage and 1.0V core voltage. The 1.0V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X112SL, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.0V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X112SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.0V.<br>During power cycle, if there is a delay in applying 1.0V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause the device totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states.<br><br>The typical time for PI7C9X112SL to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Certain precautions should be made if the delay between 3.3V and 1.0V is larger than 50us. Figure 14-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 14-2 shows the recommended power sequence timing.<br>  <br><br>**Figure** Error! No text of specified style in document.**-7 Timing sequence with undetermined I/O state**<br>  <br><br>**Figure** Error! No text of specified style in document.**-8 Recommended Power Sequence**<br>When 1.0V core power is applied after 3.3V IO power is applied, there might be glitch at reset pins (PERST_L and RESET_L), and an external RC filter can be used to filter out the glitch if necessary. | 14 POWER SEQUENCING<br>The PI7C9X112SL requires two voltages: 3.3V I/O voltage and 1.0V core voltage. The 1.0V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X112SL, the user can either apply all voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.0V) within the suggested maximum delay (50ms). If all power rails are not applied at the same time, the PI7C9X112SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.0V. |

## Current Data Sheet

### 2.2 PCI EXPRESS SIGNALS

| NAME | PIN ASSIGNMENT | TYPE | DESCRIPTION |
|---|---|---|---|
| REFCLKP<br>REFCLKN | 13, 12 | I | **Reference Clock Inputs:** Connect to external 100MHz differential clock. |
| RP<br>RN | 21, 20 | I | **PCI Express Data Inputs:** Differential data receiver input signals |
| TP<br>TN | 17, 16 | O | **PCI Express Data Outputs:** Differential data transmitter output signals |
| PERST_L | 29 | I | **PCI Express Fundamental Reset (Active LOW):** PI7C9X113SL The device uses this signal reset to initialize the internal state machines. |

## New Data Sheet

### 2.2 PCI EXPRESS SIGNALS

| NAME | PIN ASSIGNMENT | TYPE | DESCRIPTION |
|---|---|---|---|
| REFCLKP<br>REFCLKN | 13, 12 | I | **Reference Clock Inputs:** Connect to external 100MHz differential clock. These signals require AC coupled with 0.1uF capacitors. |
| RP<br>RN | 21, 20 | I | **PCI Express Data Inputs:** Differential data receiver input signals |
| TP<br>TN | 17, 16 | O | **PCI Express Data Outputs:** Differential data transmitter output signals |
| PERST_L | 29 | I | **PCI Express Fundamental Reset (Active LOW):** PI7C9X113SL The device uses this signal reset to initialize the internal state machines. |

| Current Data Sheet | New Data Sheet |
|---|---|
| 14 POWER SEQUENCING | 14 POWER SEQUENCING |
| The PI7C9X113SL requires two voltages: 3.3V I/O voltage and 1.1V core voltage. The 1.1V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X113SL, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.1V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X113SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.1V. | The PI7C9X113SL requires two voltages: 3.3V I/O voltage and 1.1V core voltage. The 1.1V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X113SL, the user can either apply all voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.1V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X113SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.1V. |
| During power cycle, if there is a delay in applying 1.1V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause PI7C9X113SL totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states. | During power cycle, if there is a delay in applying 1.1V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause PI7C9X113SL totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states. |
| The typical time for PI7C9X113SL to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Certain precautions should be made if the delay between 3.3V and 1.1V | The typical time for PI7C9X113SL to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Certain precautions should be made if the delay between 3.3V and 1.1V |

is larger than 50us. Figure 14-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 14-2 shows the recommended power sequence timing.

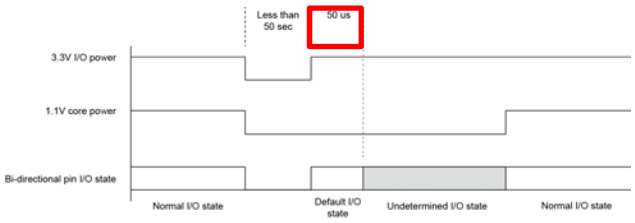



**Figure** Error! No text of specified style in document.**-9 Timing Sequence with Undetermined I/O State**

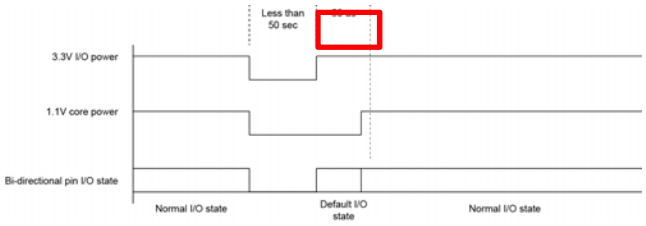



**Figure** Error! No text of specified style in document.**-10 Recommended Power Sequence**

When 1.1V core power is applied after 3.3V IO power is applied, there might be glitch at reset pins (PERST_L and RESET_L), and an external RC filter can be used to filter out the glitch if necessary.

is larger than 50us. Figure 14-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 14-2 shows the recommended power sequence timing.

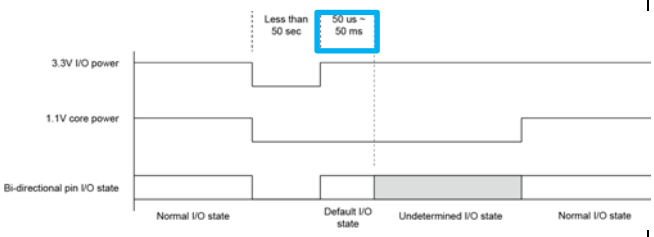



**Figure** Error! No text of specified style in document.**-11 Timing Sequence with Undetermined I/O State**

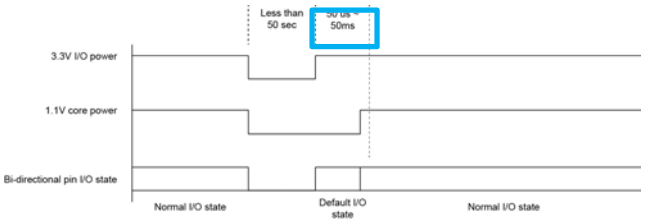



**Figure** Error! No text of specified style in document.**-12 Recommended Power Sequence**

If the gap between 3.3V IO power and 1.1V core power is too big, there might be glitch at pin RESET_L. The maximum gap is recommended to be 50us~50ms, customer needs to measure the waveform of RESET_L to make sure there is no glitch during the gap.

## Current Data Sheet

2.2 PCI EXPRESS SIGNALS

| NAME | PIN ASSIGNMENT | TYPE | DESCRIPTION |
|---|---|---|---|
| REFCLKP<br>REFCLKN | 13, 12 | I | **Reference Clock Inputs:** Connect to external 100MHz differential clock. |
| RP<br>RN | 21, 20 | I | **PCI Express Data Inputs:** Differential data receiver input signals |
| TP<br>TN | 17, 16 | O | **PCI Express Data Outputs:** Differential data transmitter output signals |
| PERST_L | 29 | I | **PCI Express Fundamental Reset (Active LOW):** PI7C9X118SL The device uses this signal reset to initialize the internal state machines. |

## New Data Sheet

2.2 PCI EXPRESS SIGNALS

| NAME | PIN ASSIGNMENT | TYPE | DESCRIPTION |
|---|---|---|---|
| REFCLKP<br>REFCLKN | 13, 12 | I | **Reference Clock Inputs:** Connect to external 100MHz differential clock. These signals require AC coupled with 0.1uF capacitors. |
| RP<br>RN | 21, 20 | I | **PCI Express Data Inputs:** Differential data receiver input signals |
| TP<br>TN | 17, 16 | O | **PCI Express Data Outputs:** Differential data transmitter output signals |
| PERST_L | 29 | I | **PCI Express Fundamental Reset (Active LOW):** PI7C9X118SL The device uses this signal reset to initialize the internal state machines. |

| Current Data Sheet | New Data Sheet |
|---|---|
| 14 POWER SEQUENCING | 14 POWER SEQUENCING |
| The PI7C9X118SL requires two voltages: 3.3V I/O voltage and 1.1V core voltage. The 1.1V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X118SL, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.1V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X118SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.1V. | The PI7C9X118SL requires two voltages: 3.3V I/O voltage and 1.1V core voltage. The 1.1V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X118SL, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.1V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X118SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.1V. |
| During power cycle, if there is a delay in applying 1.1V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause PI7C9X118SL totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states. | During power cycle, if there is a delay in applying 1.1V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause PI7C9X118SL totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states. |
| The typical time for PI7C9X118SL to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Certain precautions should be made if the delay between 3.3V and 1.1V is larger than 50us. Figure 14-1 below shows the I/O timing sequence | The typical time for PI7C9X118SL to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Certain precautions should be made if the delay between 3.3V and 1.1V is larger than 50us. Figure 14-1 below shows the I/O timing sequence |

with undetermined I/O state, and Figure 14-2 shows the recommended power sequence timing.

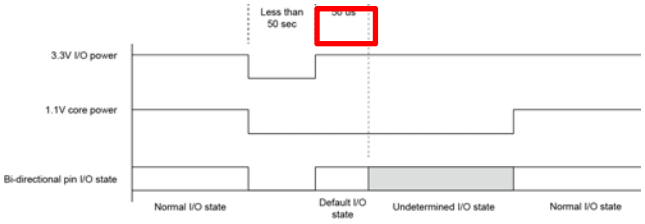



**Figure** Error! No text of specified style in document.**-13 Timing Sequence with Undetermined I/O State**

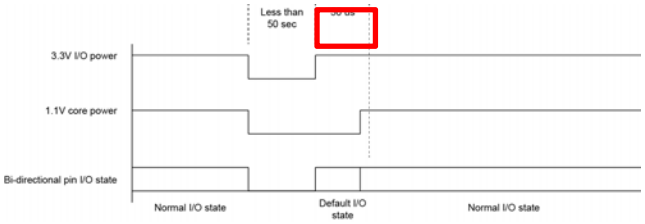



**Figure** Error! No text of specified style in document.**-14 Recommended Power Sequence**

When 1.1V core power is applied after 3.3V IO power is applied, there might be glitch at reset pins (PERST_L and RESET_L), and an external RC filter can be used to filter out the glitch if necessary.

with undetermined I/O state, and Figure 14-2 shows the recommended power sequence timing.

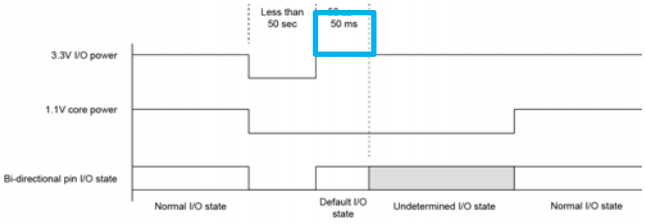



**Figure** Error! No text of specified style in document.**-15 Timing Sequence with Undetermined I/O State**

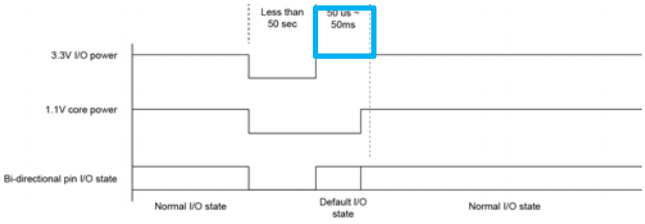
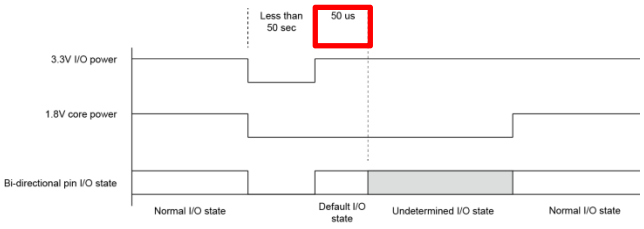
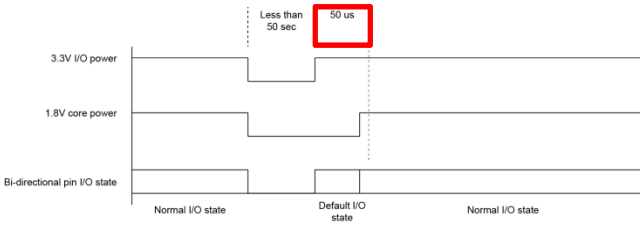
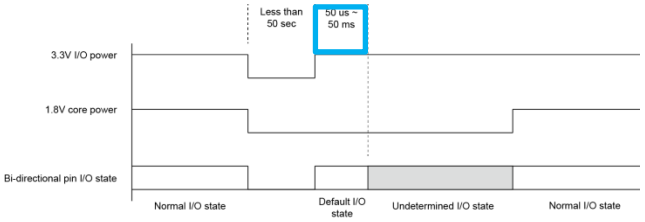
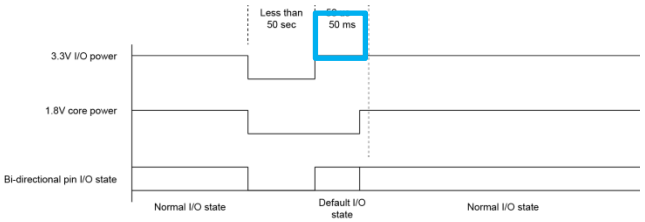



**Figure** Error! No text of specified style in document.**-16 Recommended Power Sequence**

If the gap between 3.3V IO power and 1.1V core power is too big, there might be glitch at pin RESET_L. The maximum gap is recommended to be 50us~50ms, customer needs to measure the waveform of RESET_L to make sure there is no glitch during the gap.

| Current Data Sheet | New Data Sheet |
|---|---|
| 16 POWER SEQUENCING<br>The PI7C9X130D require two voltages: 3.3V I/O voltage and 1.8V core voltage. The 1.8V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X130D, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.8V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X130D will not be damaged as long as 3.3V is applied either before or at the same time as 1.8V.<br><br>During power cycle, if there is a delay in applying 1.8V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause the device totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states.<br><br>The typical time for PI7C9X130D to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Certain precautions should be made if the delay between 3.3V and 1.8V is larger than 50us. Figure 16-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 16-2 shows the recommended power sequence timing.<br><br>  <br><br>**Figure** Error! No text of specified style in document.**-17 Timing sequence with undetermined I/O state**<br><br>  <br><br>**Figure** Error! No text of specified style in document.**-18 Recommended Power Sequence**<br><br>When 1.8V core power is applied after 3.3V IO power is applied, there might be glitch at reset pins (PERST_L and RESET_L), and an external RC filter can be used to filter out the glitch if necessary. | 16 POWER SEQUENCING<br>The PI7C9X130D require two voltages: 3.3V I/O voltage and 1.8V core voltage. The 1.8V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X130D, the user can either apply ALL voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.8V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X130D will not be damaged as long as 3.3V is applied either before or at the same time as 1.8V.<br><br>During power cycle, if there is a delay in applying 1.8V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause the device totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states.<br><br>The typical time for PI7C9X130D to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Figure 16-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 16-2 shows the recommended power sequence timing.<br><br>  <br><br>**Figure** Error! No text of specified style in document.**-19 Timing Sequence with Undetermined I/O State**<br><br>  <br><br>**Figure** Error! No text of specified style in document.**-20 Recommended Power Sequence**<br><br>If the gap between 3.3V IO power and 1.8V core power is too big, there might be glitch at pins PERST_L and RESET_L. The maximum gap is recommended to be 50us~50ms, customer needs to measure the waveform of PERST_L and RESET_L to make sure there is no glitch during the gap. |